DYNAMIC POWER DISSIPATION METHODS FOR FPGA DEVICES

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Field-Programmable Gate Array (FPGA) devices are one of the most popular choice for medium to high volume density digital applications. They can be used in various implementations for different circuits without the need of fabrication of a new chip, reducing costs. Such flexibility in design is paid for by increased power dissipation. The power consumed by a logic circuit implemented on an FPGA device especially in a 90nm, or smaller, is to be used in a mobile application. In this work we are concerned strictly with the dynamic power dissipated by a logic circuit. The purpose of these changes is to improve a previously synthesized circuit to reduce the amount of dissipated dynamic power. Furthermore, we show how to take advantage of post-routing information to achieve power reduction. In this chapter a method for reducing the dynamic power dissipated by Field-Programmable Gate Array is presented. This method uses a probabilistic approach for detecting glitches in a fully placed and routed circuit and then applies a glitch reduction technique that uses negative edge-triggered flip-flops to reduce the number of glitches in a logic circuit. The key idea behind the glitch reduction technique is to insert negative-edge-triggered flip-flops at outputs of Lookup Tables that produce glitches. It maintains the logic value produced by the LUT in the previous clock cycle for the first half of the clock period, filtering glitches that occur at the output of the LUT. This method reduces the number of logic value transitions that propagate to the general routing network, thereby reducing the dynamic power dissipated by a logic circuit.

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